

### General Description

The AAT7157 low threshold 20V, dual P-channel MOSFET is a member of AnalogicTech's TrenchDMOS product family. Using an ultra-high density proprietary TrenchDMOS technology, the AAT7157 is designed for use as a load switch in battery-powered applications and protection in battery packs.

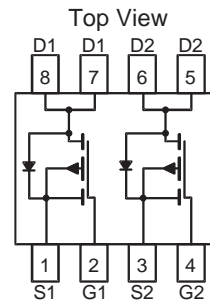
### Features

- $V_{DS(MAX)} = -20V$
- $I_{D(MAX)}^1 = -5.8A @ 25^{\circ}C$
- Low  $R_{DS(ON)}$ :
  - $36m\Omega @ V_{GS} = -4.5V$
  - $62m\Omega @ V_{GS} = -2.5V$

### Applications

- Battery Packs
- Battery-Powered Portable Equipment

### Dual SOP-8L Package



### Absolute Maximum Ratings

$T_A = 25^{\circ}C$ , unless otherwise noted.

Symbol	Description	Value	Units
$V_{DS}$	Drain-Source Voltage	-20	V
$V_{GS}$	Gate-Source Voltage	$\pm 12$	
$I_D$	Continuous Drain Current @ $T_J = 150^{\circ}C^1$	$T_A = 25^{\circ}C$	$\pm 5.8$
		$T_A = 70^{\circ}C$	$\pm 4.6$
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	$\pm 24$	A
$I_S$	Continuous Source Current (Source-Drain Diode) <sup>1</sup>	-1.5	
$P_D$	Maximum Power Dissipation <sup>1</sup>	$T_A = 25^{\circ}C$	2.0
		$T_A = 70^{\circ}C$	1.25
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^{\circ}C$

### Thermal Characteristics

Symbol	Description	Value	Units
$R_{\theta JA}$	Typical Junction-to-Ambient Steady State <sup>1</sup>	100	$^{\circ}C/W$
$R_{\theta JA2}$	Maximum Junction-to-Ambient t<10 Seconds <sup>1</sup>	62.5	
$R_{\theta JF}$	Typical Junction-to-Foot <sup>1</sup>	35	

1. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 10-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications.  $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$  where the foot thermal reference is defined as the normal solder mounting surface of the device's leads.  $R_{\theta JF}$  is guaranteed by design; however,  $R_{\theta CA}$  is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

2. Pulse test: Pulse Width = 300 $\mu s$ .

### Electrical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>DC Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
$R_{DS(ON)}$	Drain-Source On-Resistance <sup>1</sup>	$V_{GS} = -4.5V, I_D = -5.8A$		29	36	m $\Omega$
		$V_{GS} = -2.5V, I_D = -4.4A$		49	62	
$I_{D(ON)}$	On-State Drain Current <sup>1</sup>	$V_{GS} = -4.5V, V_{DS} = 5V$ (Pulsed)	-24			A
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu A$	-0.6			V
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS} = \pm 12V, V_{DS} = 0V$			$\pm 100$	nA
$I_{DSS}$	Drain Source Leakage Current	$V_{GS} = 0V, V_{DS} = -20V$			-1	$\mu A$
		$V_{GS} = 0V, V_{DS} = -16V, T_J = 70^\circ\text{C}^2$			-5	
$g_{fs}$	Forward Transconductance <sup>1</sup>	$V_{DS} = -5V, I_D = -5.8A$		12		S
<b>Dynamic Characteristics<sup>2</sup></b>						
$Q_G$	Total Gate Charge	$V_{DS} = -15V, R_D = 2.6\Omega, V_{GS} = -4.5V$		14		nC
$Q_{GS}$	Gate-Source Charge	$V_{DS} = -15V, R_D = 2.6\Omega, V_{GS} = -4.5V$		2.3		
$Q_{GD}$	Gate-Drain Charge	$V_{DS} = -15V, R_D = 2.6\Omega, V_{GS} = -4.5V$		5.5		
$t_{D(ON)}$	Turn-On Delay	$V_{DS} = -15V, R_D = 2.6\Omega, V_{GS} = -4.5V, R_G = 6\Omega$		10		ns
$t_R$	Turn-On Rise Time	$V_{DS} = -15V, R_D = 2.6\Omega, V_{GS} = -4.5V, R_G = 6\Omega$		37		
$t_{D(OFF)}$	Turn-Off Delay	$V_{DS} = -15V, R_D = 2.6\Omega, V_{GS} = -4.5V, R_G = 6\Omega$		36		
$t_F$	Turn-Off Fall Time	$V_{DS} = -15V, R_D = 2.6\Omega, V_{GS} = -4.5V, R_G = 6\Omega$		52		
<b>Source-Drain Diode Characteristics</b>						
$V_{SD}$	Source-Drain Forward Voltage <sup>1</sup>	$V_{GS} = 0, I_S = -5.8A$			-1.5	V
$I_S$	Continuous Diode Current <sup>3</sup>				-1.5	A

1. Pulse test: Pulse Width = 300 $\mu s$ .

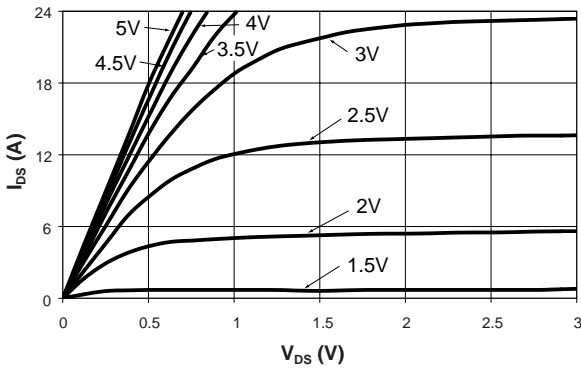
2. Guaranteed by design. Not subject to production testing.

3. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 10-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications.  $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$  where the foot thermal reference is defined as the normal solder mounting surface of the device's leads.  $R_{\theta JF}$  is guaranteed by design; however,  $R_{\theta CA}$  is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

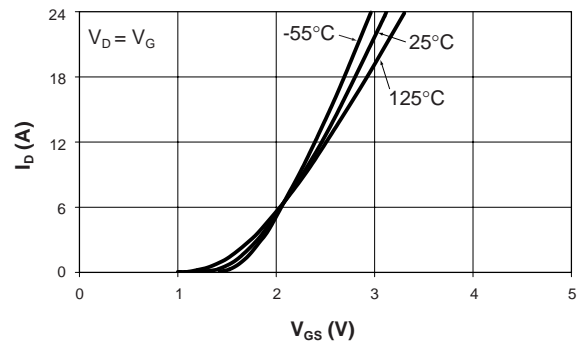
## Typical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

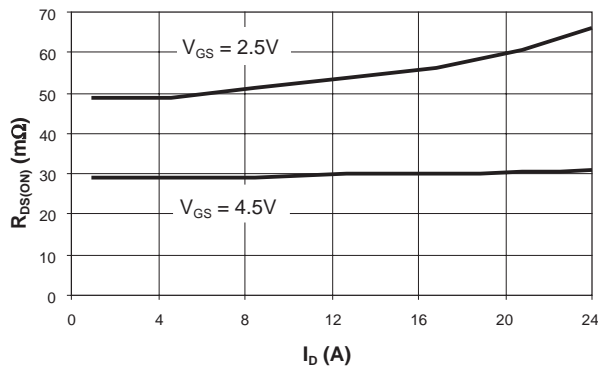
**Output Characteristics**



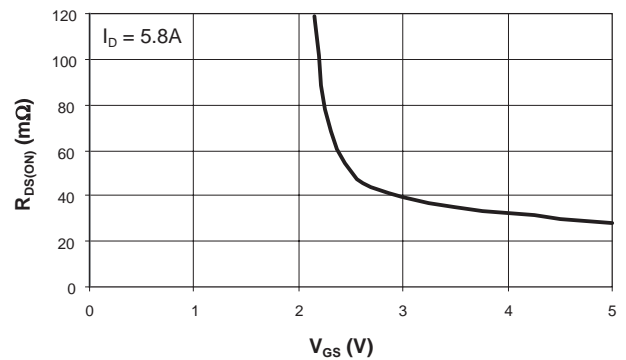
**Transfer Characteristics**



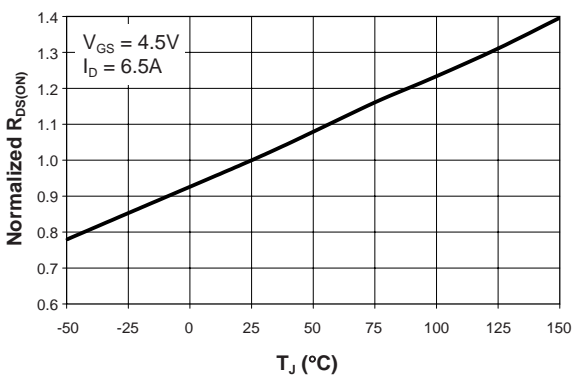
**On-Resistance vs. Drain Current**



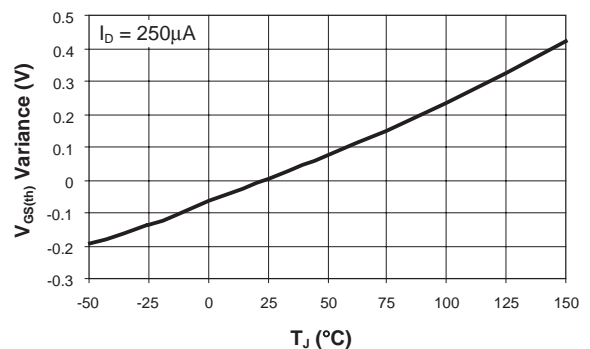
**On-Resistance vs. Gate-to-Source Voltage**



**On-Resistance vs. Junction Temperature**



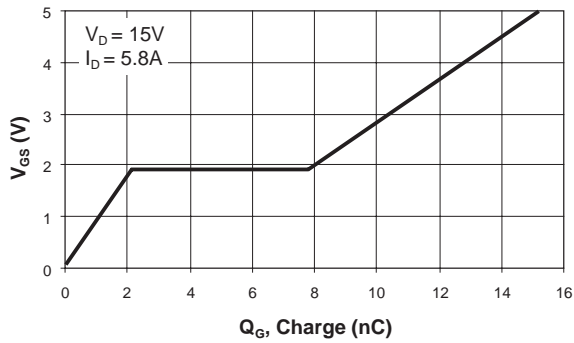
**Threshold Voltage**



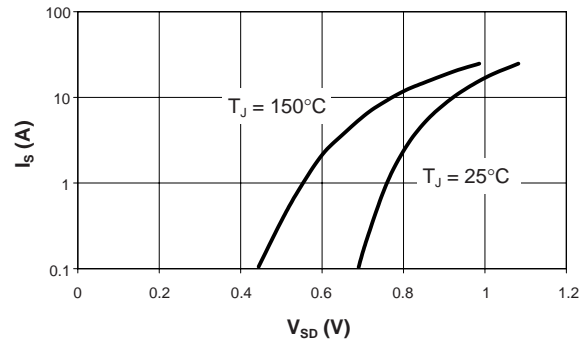
## Typical Characteristics

$T_J = 25^\circ\text{C}$ , unless otherwise noted.

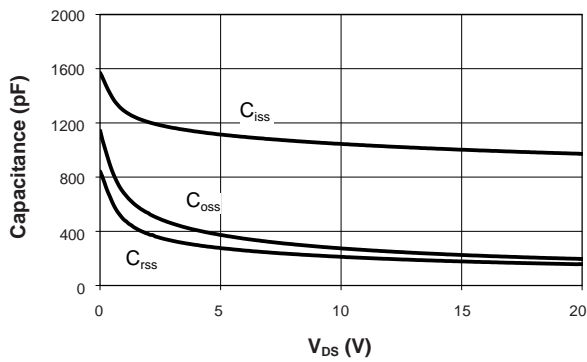
**Gate Charge**



**Source-Drain Diode Forward Voltage**



**Capacitance**

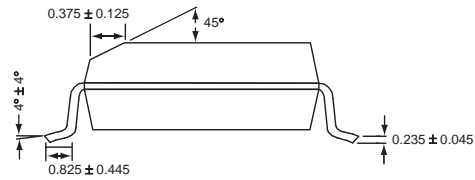
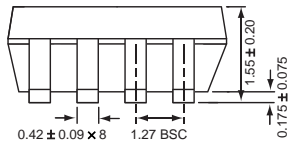
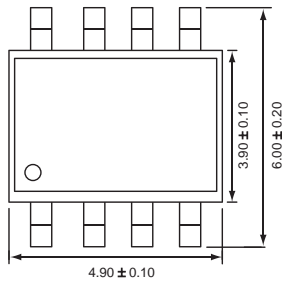


### Ordering Information

Package	Marking	Part Number (Tape and Reel) <sup>1</sup>
SOP-8	7157	<b>AAT7157IAS-T1</b>

### Package Information

#### SOP-8



All dimensions in millimeters.

1. Sample stock is generally held on all part numbers listed in **BOLD**.

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